# Persistent Memory Objects on the Cheap

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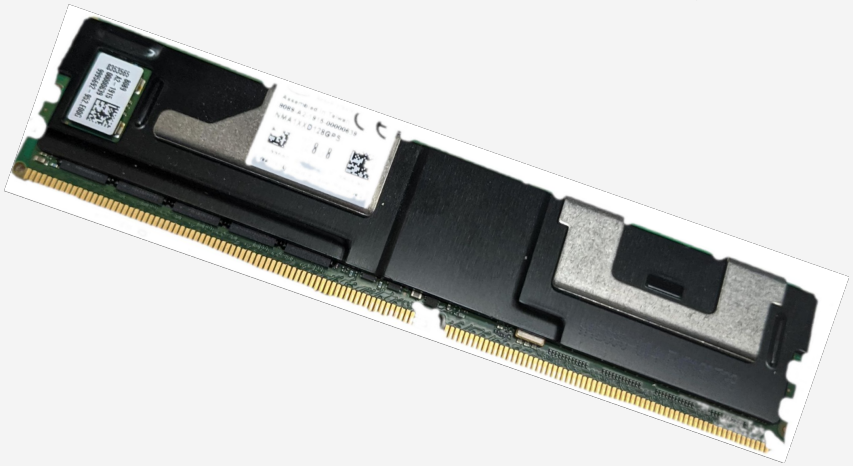
# Overview

# Persistent Memory (PM)

Example: Intel Optane, CXL Memory-Semantic SSDs



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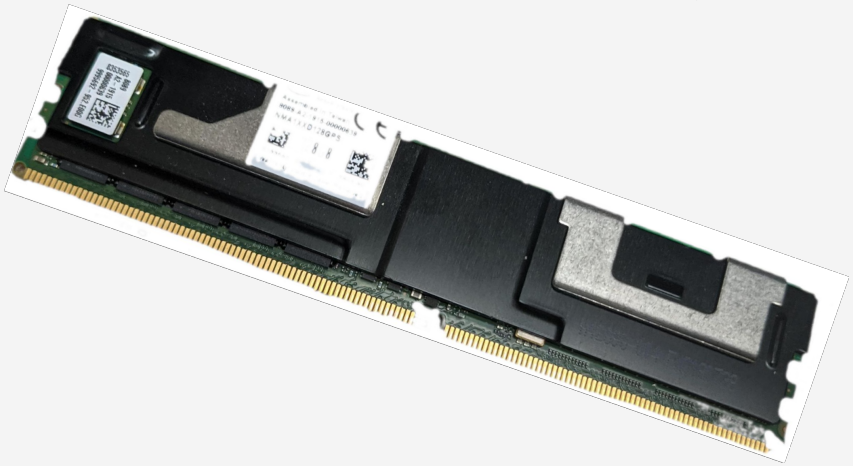

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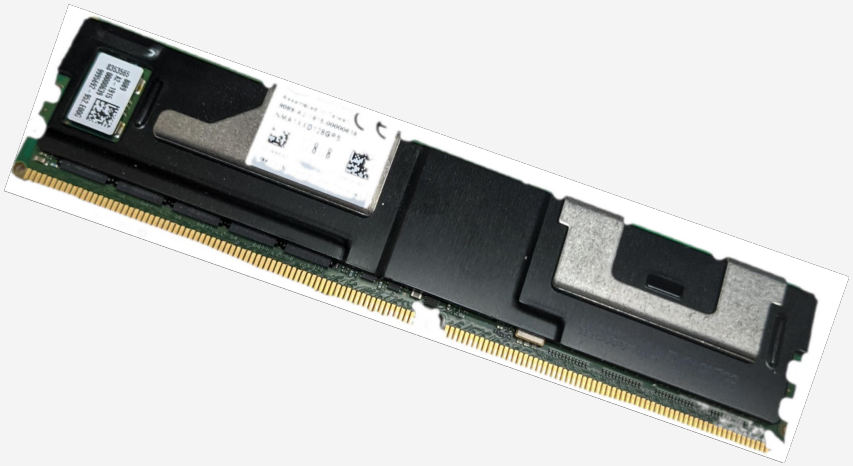

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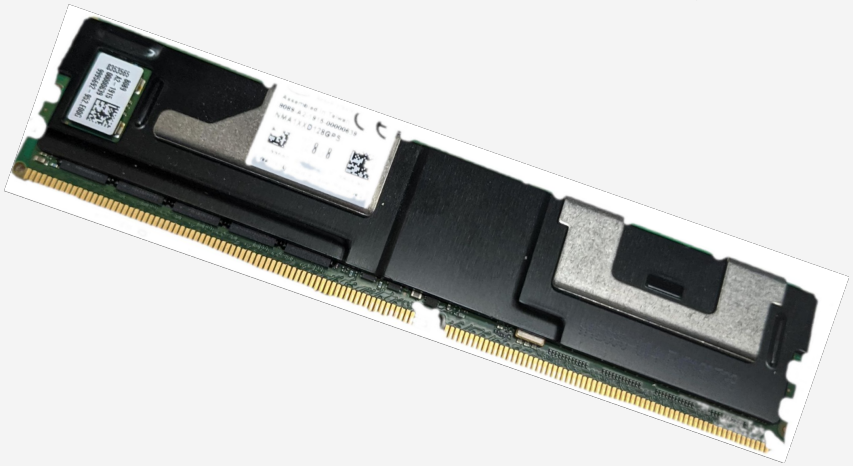

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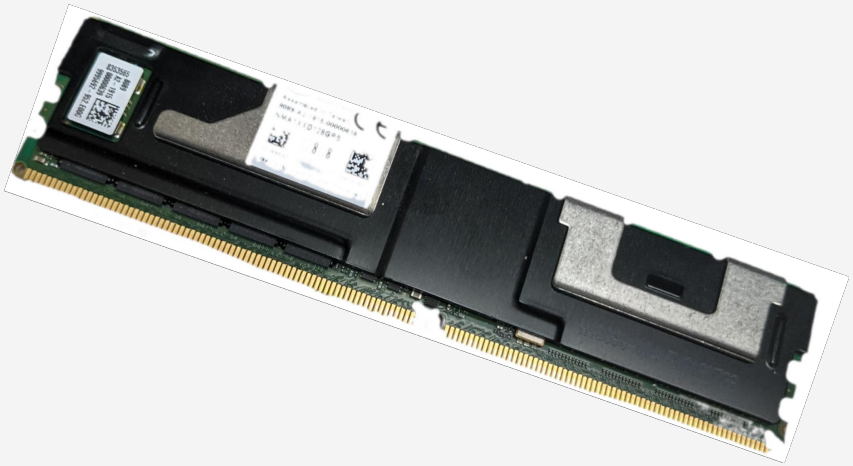

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Note: Devices with PM usually have DRAM as well


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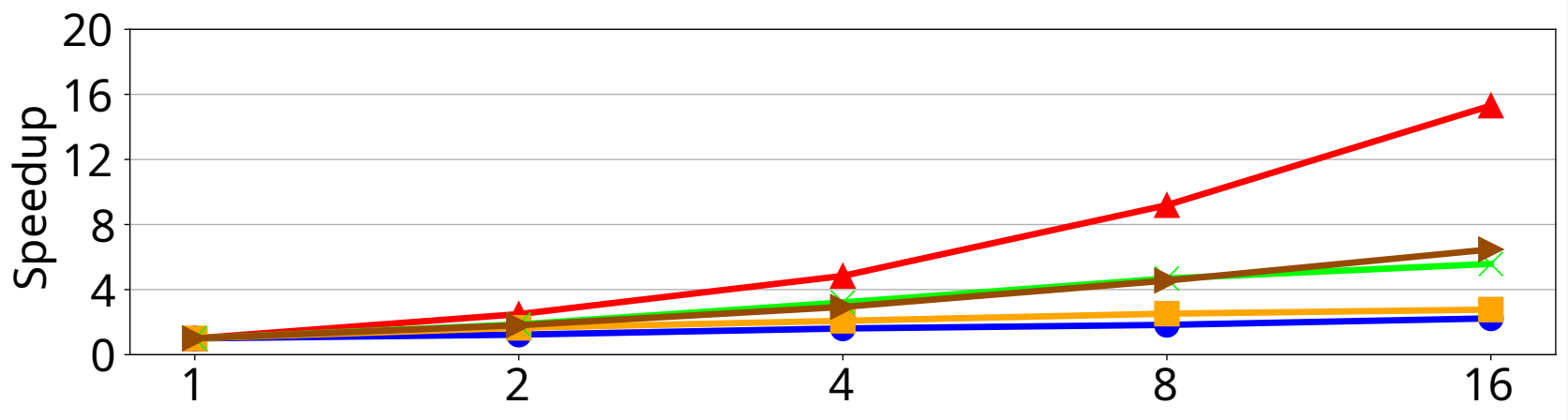

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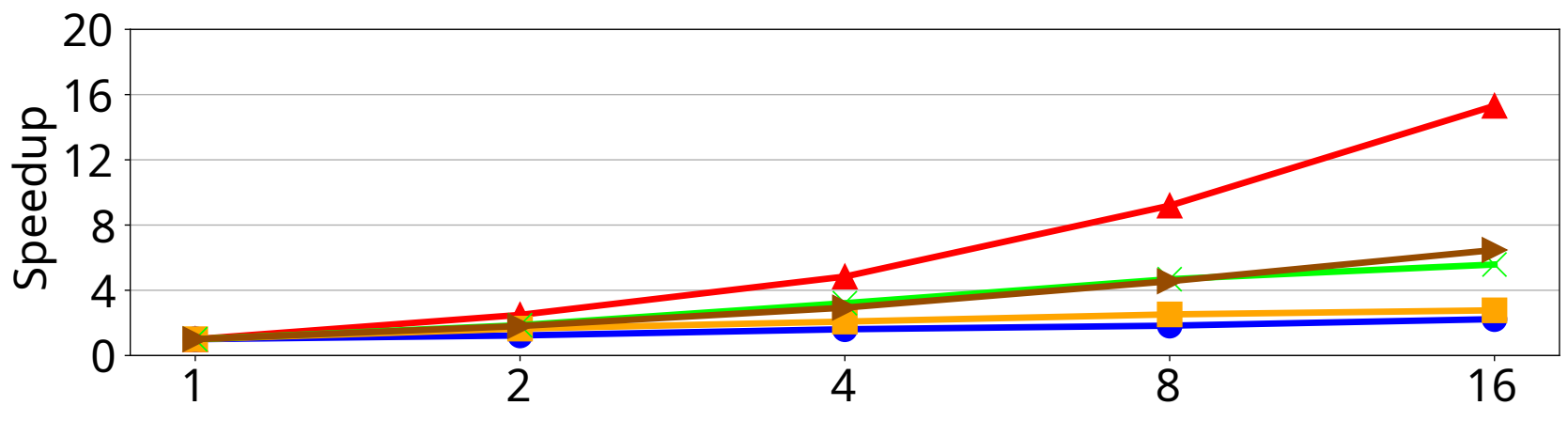


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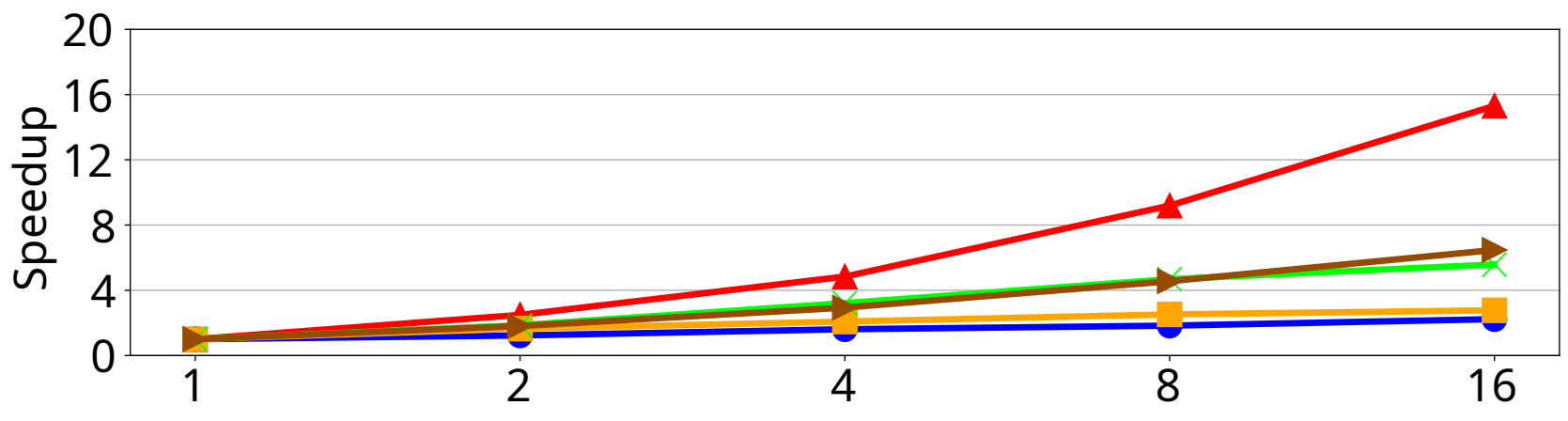


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- Encryption and integrity verification on the critical path


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**Goal: High-Performance PMOs**


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...more on this later.


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# Threat Model

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## Out of Scope

- Side-channel attacks
- Data-remanence attacks (DRAM)


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DRAM as cache = Reconfigurable Memory


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- **Shadow in plaintext, primary in ciphertext**


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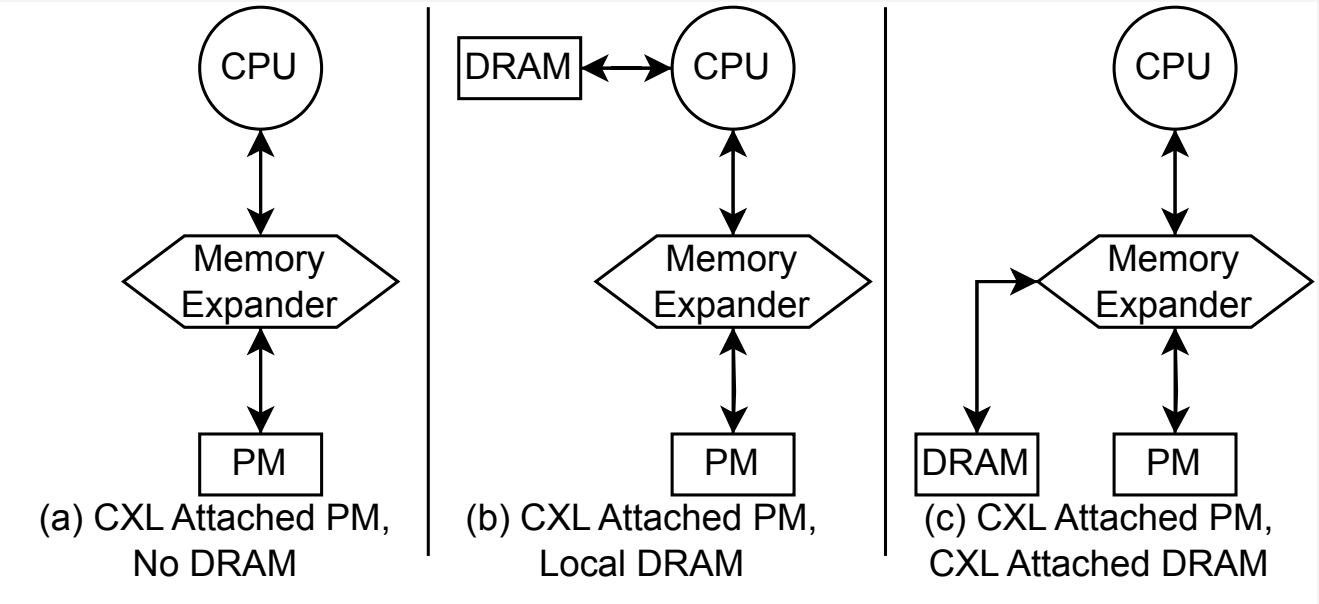


CXL can place system on either side of memory expander


# Reduce page fault latency

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## Example Solution: Stream Buffer

- On fault, predict next $X$ sequential pages (**depth**)
- Works well for access patterns amenable to prediction


# Overview


# Evaluation

## Evaluated Benchmarks

- Microbenchmarks
  - 2d Convolution (2dConv)
  - Gaussian Elimination (Gauss)
  - LU Decomposition (LU)
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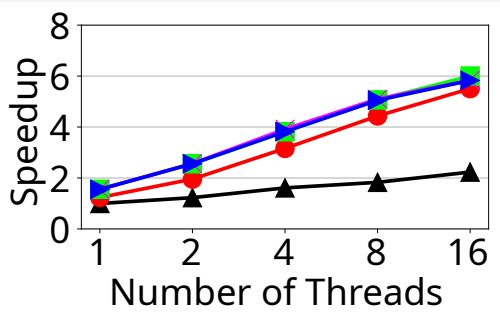
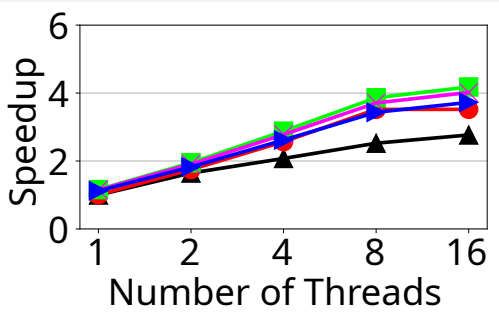
| Component | Specifications |
|---|---|
| MB | Supermicro X11DPi-NT |
| CPU | 2×Intel Xeon Gold 6230 (20 cores) |
| DRAM | 4 × 32GiB DDR4 @ 2666MHz |
| PM | 4 × 128GiB Intel Optane DIMM |
| OS | AlmaLinux 9.0; Linux 5.15.157 |

# LPMO Performance

△ O, ○ D, □ D2, × D4, ▷ D8




(a) Gauss

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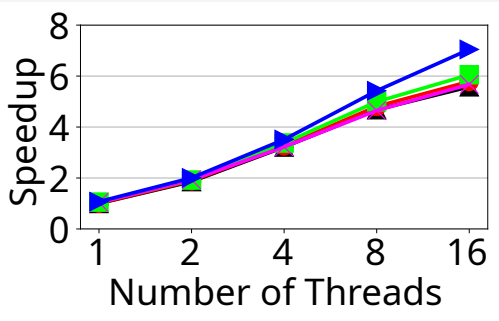


(c) TMM

All benchmarks have better thread scaling!

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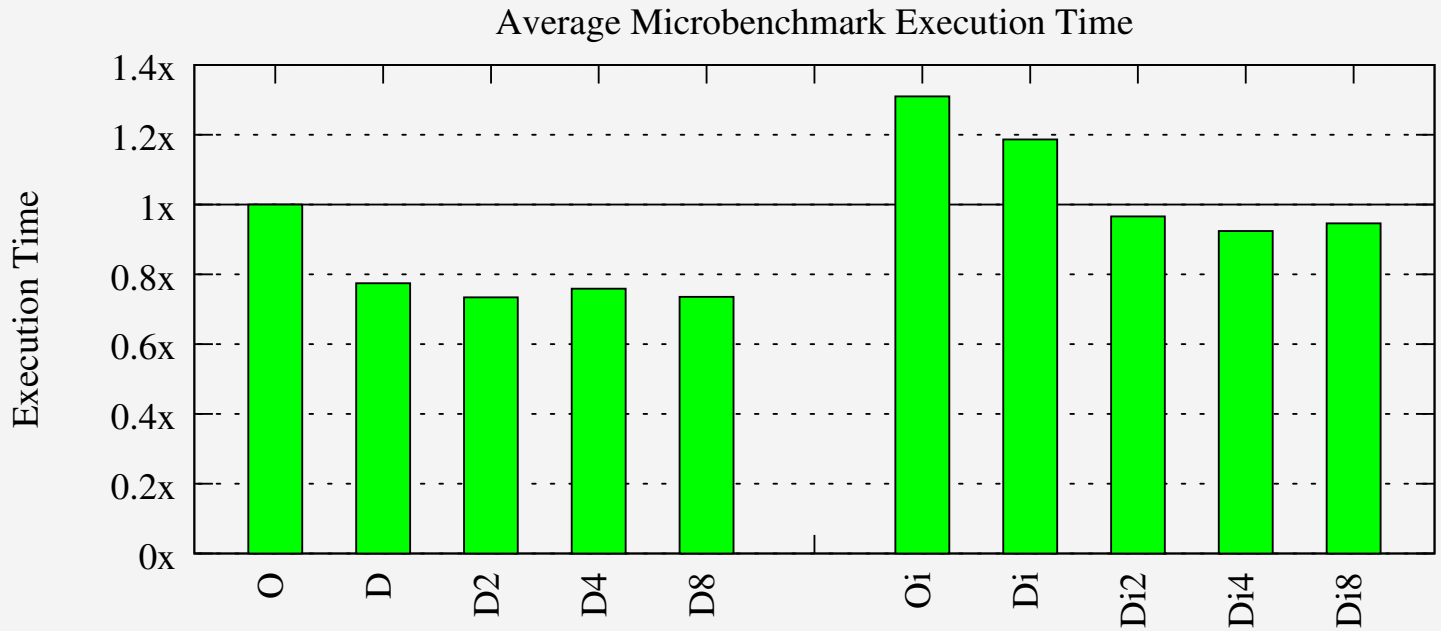


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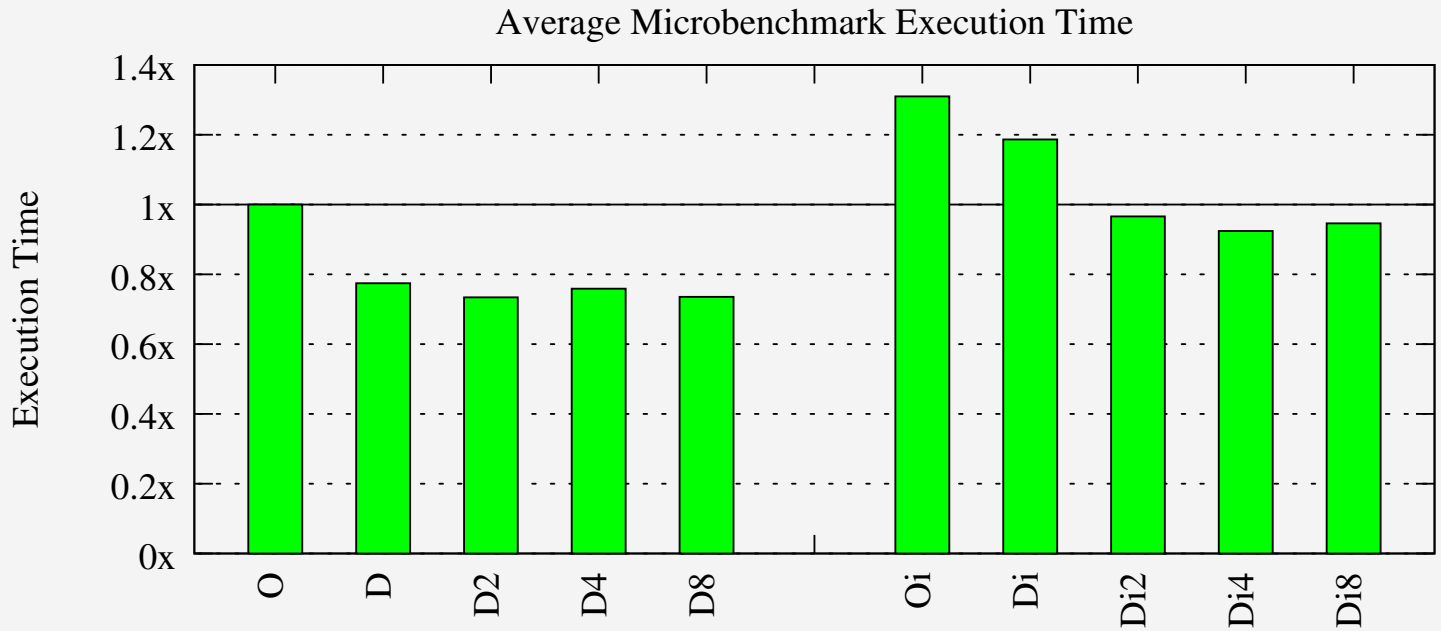
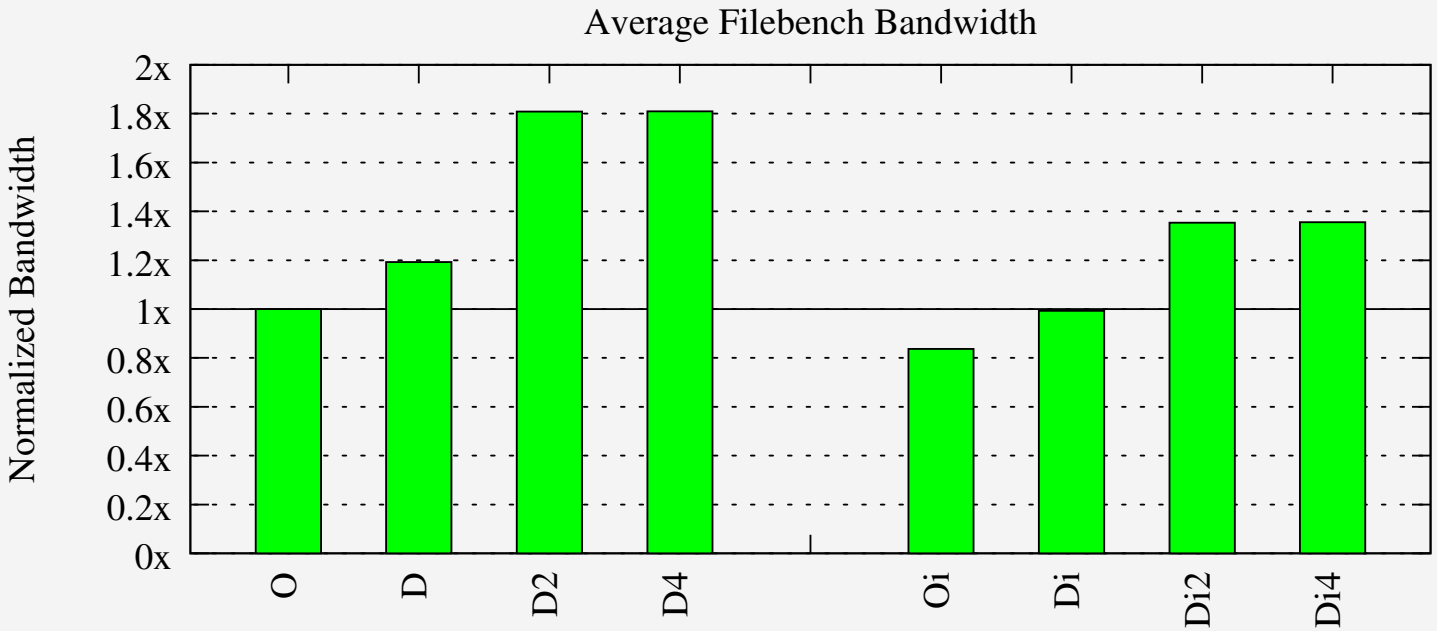



- DRAM reduces execution time by $\approx 21\%$
- IV + Prediction faster than original GPMO design w/o IV

# LPMO Performance - Filebench

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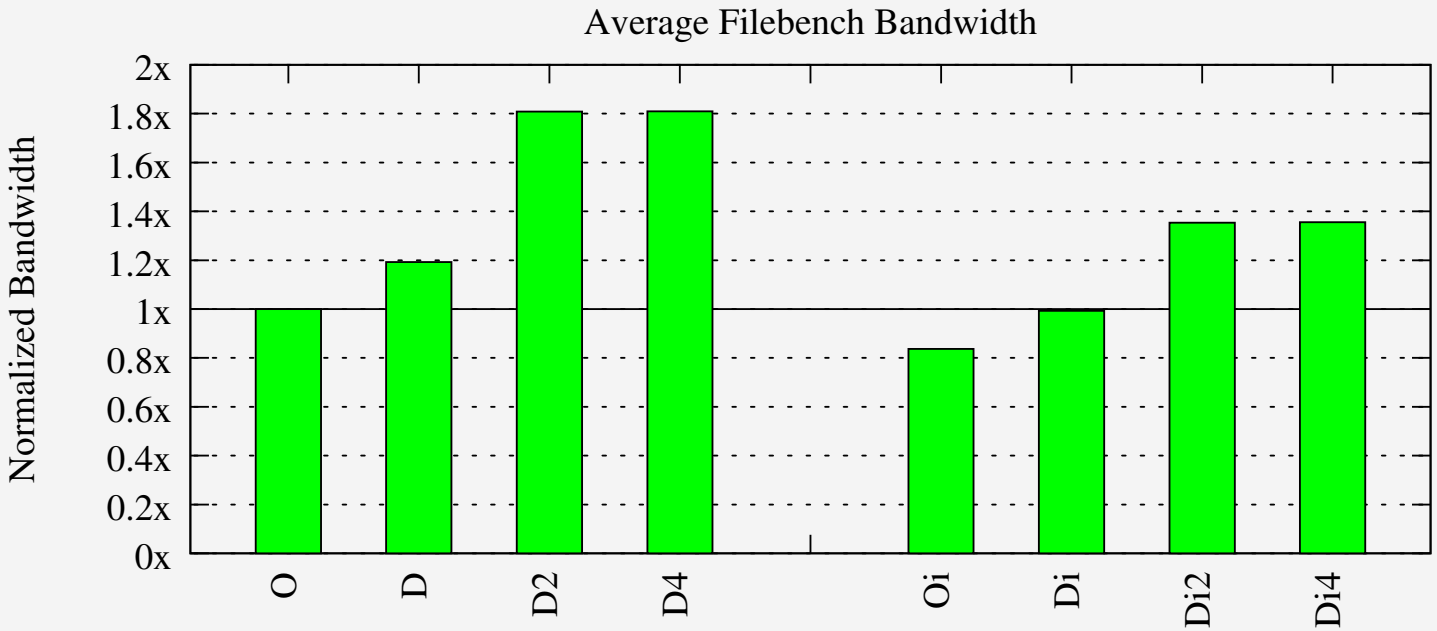


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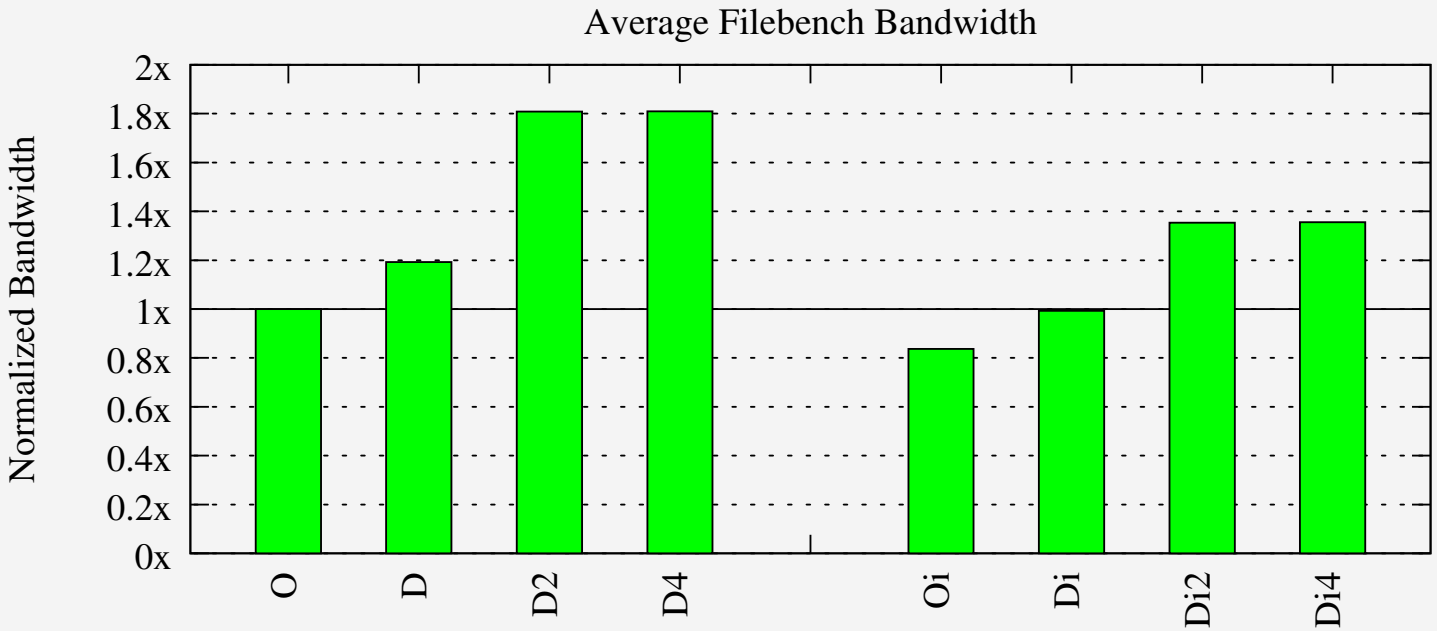


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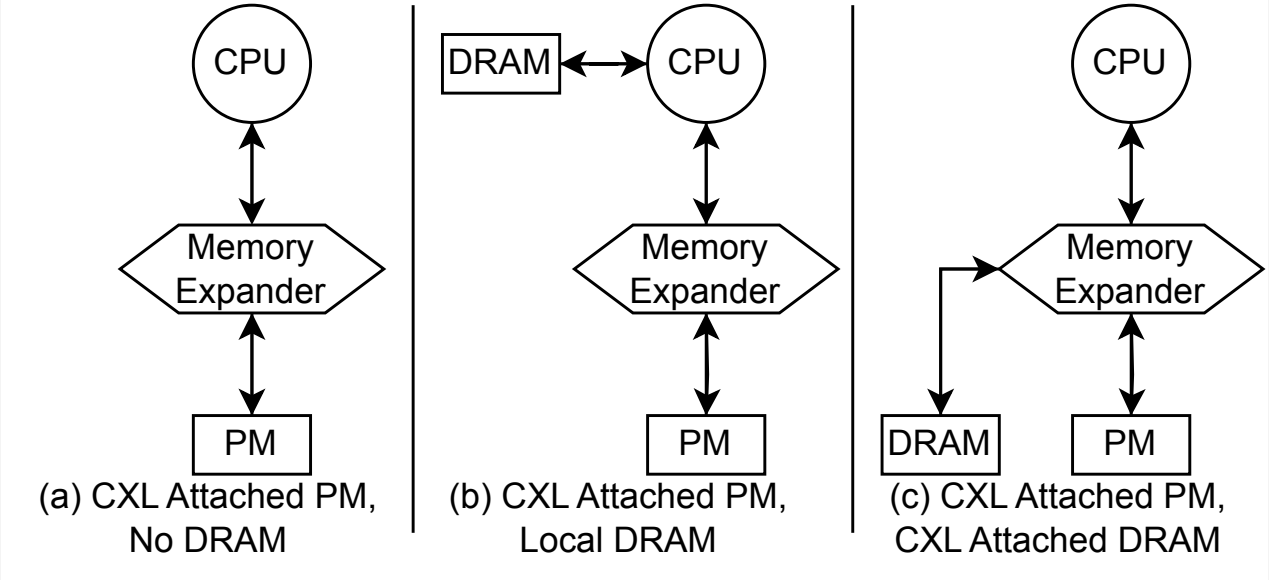
- 1.37× faster with page prediction & **IV**

# CXL Performance

Perform same tests, but emulate CXL latency




- Use opposite-node Optane
- Near configuration: cache allocated from local node
- Far configuration: cache allocated from opposite node

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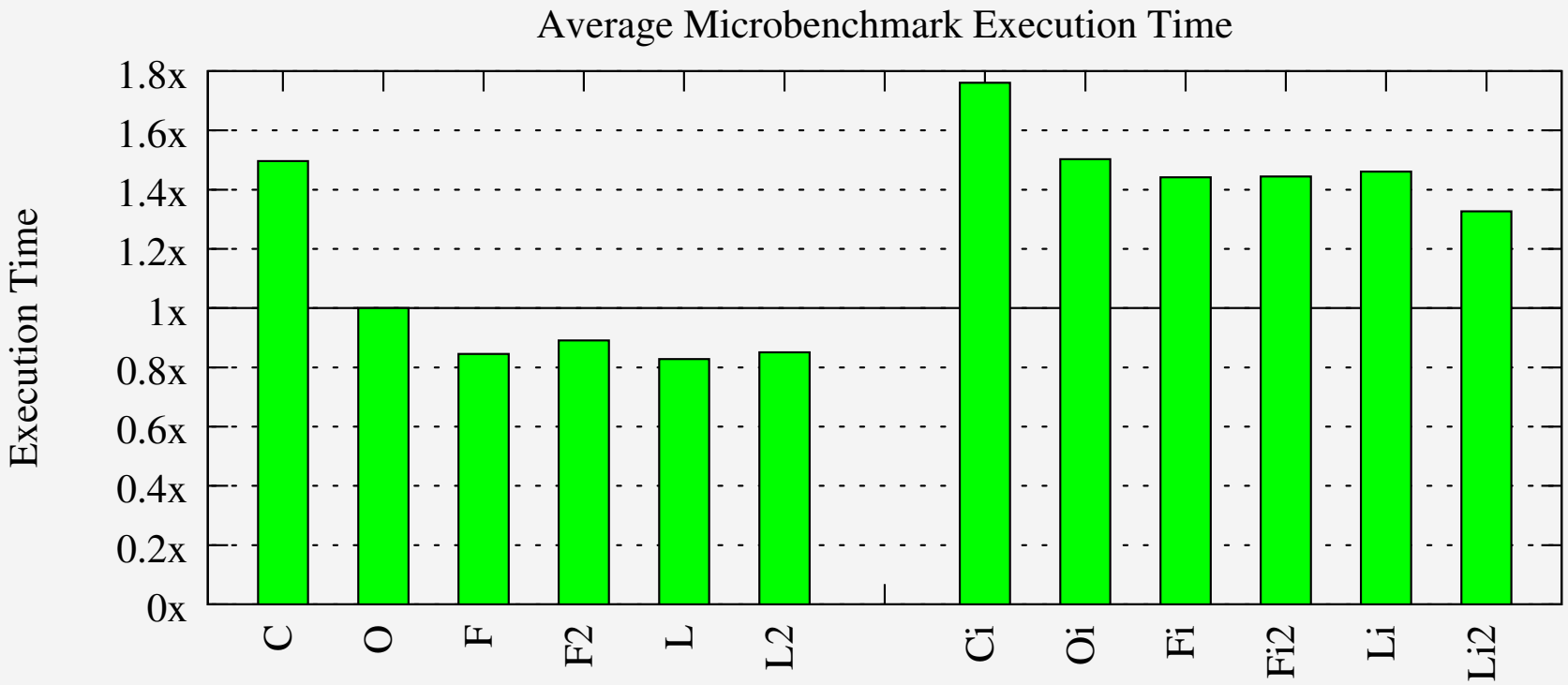


(Lower is better)

- With CXL alone: 50% slower than original
- With DRAM: 20% faster (despite CXL latency)

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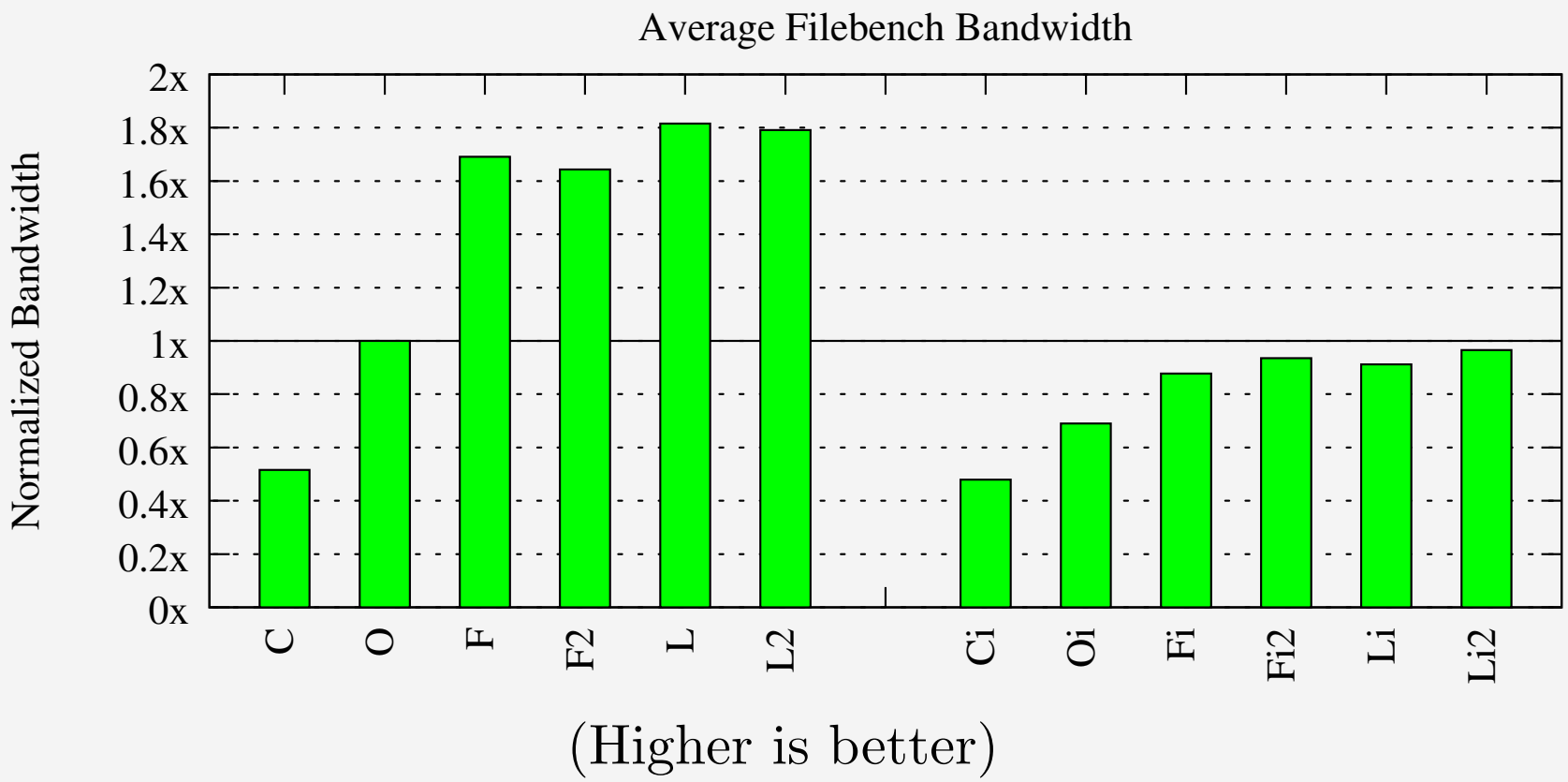


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## CXL

- Introduced Reconfigurable Memory Hierarchy
- CXL latency can be masked by LPMO optimizations


# Q & A

**Thank You!**

Any questions?